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EXAMINER	
JEAN GILLES, JUDE	

ART UNIT	PAPER NUMBER
2143	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/896,563	HAMILTON ET AL.	
	Examiner	Art Unit	
	JUDE J. JEAN GILLES	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in Reply to the Reply received on 03/31/2008.

Response to Amendment/Arguments

1. Applicant's arguments filed 03/31/2008 have been fully considered but they are not persuasive. Claims 17-40 are pending and represent a "METHOD TO PROVIDE DIRECT SYSTEM STORAGE ACCESS WITHIN A NOTEBOOK COMPUTER VIA A WIRELESS INTERCONNECT AND A LOW POWER HIGH-SPEED DATA MANAGEMENT BUS WHILE THE MAIN CPU IS IDLE.

2. Applicants' arguments are moot in view of the existing grounds of rejection presented in the previous Office Action. Because it is likely that the same arguments will be presented in the future, the Examiner finds it prudent to address applicants' main points of contention.

Applicants contend that claim 17 calls for activating an idle storage device on a computer system while a main processor of that computer system remains idle. Thus, the storage device must be activated while the processor remains idle. This does not happen in the cited reference to Kostadinov. In Kostadinov, a selector device activates the previously inactivate memory area "by directing the microprocessor to the entry points of the newly-downloaded executable instructions or data". *See* paragraph 56, the 9-11th lines from the end of the paragraph. Then the memory activation must occur while the processor is not performing application execution, etc. By so timing the memory activation, a processor may be redirected without microprocessor interruption.

It is clear from the cited material that the processor is used to activate the memory area. Therefore, the processor cannot be idle. The reference suggests that the processor not be doing some other task at the time it activates the idle storage so that the microprocessor is not interrupted. But by using the microprocessor explicitly by directing the microprocessor to entry points, the microprocessor necessarily cannot be idle at the critical time. The critical time is when the storage device is activated.

The Examiner disagrees with Applicants assertion of the teachings of Kostadinov. In Kostadinov Par. 0056 and the abstract of the invention discloses without ambiguity that the memory activation must occur while the microprocessor is not performing application execution, application input/output, or application communications...and it is conceivable that the microprocessor is idle as it is inactive, not performing any tasks while the memory, the storage device being activated for data transfer. The rejections under 35 U.S.C. 103(a) are therefore sustained.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 17-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kostadinov, U.S. Pub. 2007/0234339 A1 in view of Mishler, U.S. Patent No 5,283,883.

Regarding **claim 17**, Kostadinov teaches the invention substantially as claimed. Kostadinov discloses a method, comprising:

activating an idle storage device in a computer system to transfer data while a main processor of the computer is idle (*Abstract; see that …the memory activation must occur while the microprocessor is not performing application execution, application input/output, or application communications...and it is conceivable that the microprocessor is idle as it is inactive, not performing any tasks while the memory, the storage device being activated for data transfer; see also par. 0056*);

executing the data transfer (see abstract, see also par. 0056).

Although Kostadinov teaches substantial features of the claimed invention, Kostadinov does not distinctly disclose "returning system resources to an idle state". Nonetheless this feature is well known and would have been an obvious modification to the system shown by Kostadinov as evidenced by Mishler.

In an analogous art, Mishler shows a Direct Memory Access (DMA) Controller capable of activating and deactivating system resources. Specifically, Mishler teaches a method of transferring data bytes out of the memory, and upon a completion of the data bytes transfer from the memory to one of the buffer lines, returns the system's resources to the idle state (see Mishler, column 11, lines 21-26).

Given this feature, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the system shown Kostadinov to employ the features shown by Mishler in order to facilitate cooperative asynchronous reading and writing of data into a system's plurality of elements (see Mishler, column 2, lines 11-13). DMA controllers are used to help control access to system's memory resources as demonstrated by the system of Mishler. By this rationale, claim 17 is rejected.

18. (Previously Presented) The method of claim 17, further comprising:
buffering the data for transfer (see Mishler, column 2, lines 1-13). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

19. (Previously Presented) The method of claim 17, further comprising:
detecting a request for data transfer to activate the idle storage device while the main processor of the computer is idle (see Kostadinov, abstract, see also par. 0056).

20. (Previously Presented) The method of claim 19, wherein a controller activates the idle storage device by directing power to the device (see Mishler, fig. 1, item 20). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

21. (Previously Presented) The method of claim 17, further comprising:

tagging the transferred data for recognition (see Kostadinov, abstract, see also par. 0056).

22. (Previously Presented) The method of claim 17, further comprising:
apportioning a system time and power resource based on the transferred data (see Kostadinov, abstract, see also par. 0056).

23. (Previously Presented) The method of claim 22, further comprising:
returning the system resource to a pre-transfer state (see Mishler, column 11, lines 21-26).

24. (Previously Presented) The method of claim 17, further comprising:
notifying a user of the computer system of the data transfer after the system is returned to an idle state (see Kostadinov, par. 0037; 0056).

25. (Previously Presented) The method of claim 17, wherein the data is transferred wirelessly (see Kostadinov, par. 0006; note that the Fieldbus can be used to transfer data within a wireless LAN).

26. (Previously Presented) The method of claim 17, wherein the data is transferred via a low level data bus (see Kostadinov, see fig. 1).

27. (Previously Presented) An apparatus comprising:

means for activating an idle storage device in a computer system to transfer data while a main processor of the computer is idle (see Kostadinov, abstract, see also par. 0056);

means for executing the data transfer (see Kostadinov, abstract, see also par. 0056); and

means for returning system resources to an idle state (see Mishler, column 11, lines 21-26).

28. (Previously Presented) The apparatus of claim 27, further comprising:

means for buffering the data for transfer (see Mishler, column 2, lines 1-13). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

29. (Previously Presented) The apparatus of claim 27, wherein the means for activating the idle storage device comprise a controller that detects a request for data transfer while the main processor of the computer is idle (see Mishler, fig. 1, item 20). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

30. (Previously Presented) The apparatus of claim 29, wherein the controller activates the idle storage device by directing power to the device (see Mishler, fig. 1, item 20).

The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

31. (Previously Presented) The apparatus of claim 27, wherein the data is transferred wirelessly (see Kostadinov, par. 0006; note that the Fieldbus can be used to transfer data within a wireless LAN).

32. (Previously Presented) The apparatus of claim 27, wherein the data is transferred via a low level data bus (see Kostadinov, see fig. 1).

33. (Previously Presented) A machine-readable medium having executable instructions to cause a processor to perform a method, the method comprising:
activating an idle storage device in a computer system to transfer data while a main processor of the computer is idle (see Kostadinov, abstract, see also par. 0056);
executing the data transfer (see Kostadinov, abstract, see also par. 0056); and
returning system resources to an idle state (see Mishler, column 11, lines 21-26).

34. (Previously Presented) The machine-readable medium of claim 33, wherein the method further comprises:
buffering the data for transfer (see Mishler, column 2, lines 1-13). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

35. (Previously Presented) The machine-readable medium of claim 34, wherein the idle storage device is activated by a controller that detects a request for data transfer while the main processor of the computer is idle (see Mishler, fig. 1, item 20). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

36. (Previously Presented) The machine-readable medium of claim 33, wherein the method further comprises:
apportioning a system resource based on the transferred data (see Kostadinov, abstract, see also par. 0056).

37. (Previously Presented) The machine-readable medium of claim 36, wherein the method further comprises:
returning the system resource to a pre-transfer state (see Mishler, column 11, lines 21-26).

38. (Previously Presented) A computer system comprising:
a processor coupled to a memory through a bus (see Kostadinov, fig. 1);
a unit to activate a storage device in a computer system to transfer data while the processor is idle, the unit to execute the data transfer (see Kostadinov, abstract, see also par. 0056), and the unit to
return system resources to an idle state (see Mishler, column 11, lines 21-26).

39. (Previously Presented) The system of claim 38, further including a buffer to store data to be transferred (see Mishler, column 2, lines 1-13). The same motivation and reason to combine utilized for the rejection of claim 17 is also valid for this claim.

40. (Previously Presented) The system of claim 38, further including a unit to detect a request for data transfer to activate the idle storage device while the main processor of the computer is idle (see Kostadinov, abstract, see also par. 0056).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from examiner should be directed to Jude Jean-Gilles whose telephone number is (571) 272-3914. The examiner can normally be reached on Monday-Thursday and every other Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3301.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-0800.

/Jude J Jean-Gilles/

Primary Examiner, Art Unit 2143

JJG

June 30, 2008

/Nathan J. Flynn/

Supervisory Patent Examiner, Art Unit 2154